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| 09/430,350 | 10/29/1999 | MASSIMO SUTERA | P4158/PJM | 7163 |

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| EXAMINER |
|---|
| JONES, HUGH M |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2123 | |

DATE MAILED: 02/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

NM

| Office Action Summary | Application No. 09/430,350 | Applicant(s) Sutera et al. |
|---|---|---|
| | Examiner Hugh Jones | Art Unit 2123 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on *Oct 29, 1999*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-4* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Oct 29, 1999* is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

## DETAILED ACTION

### *Information Disclosure Statement*

1. Applicants have not provided an IDS. The Examiner notes that while the alleged deficiencies of prior art have been discussed in the specification (see section 2 ["the backround art"] of the specification, for example), and Applicants have admitted that the concepts expressed in figure 2 are prior art, there has been no mention, in an IDS, of such prior art. As these references are not readily available to the Examiner, the applicant should provide the office with copies of the reference in any response to this action.

2. Applicant is **reminded** of their duty to disclose all information material to the patentability of the application as per 37 C.F.R. 1.56.

### *Drawings*

3. Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. Note the caption for figure 2 on page 3. See MPEP § 608.02(g).

### *Claim Rejections - 35 USC § 101*

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. **Claims 2 and 4 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.** Claims 2 and 4 recite a computer program product. It should be noted that code (i.e., a computer software program) does not do anything per se. Instead, it is the code stored on a computer that, *when executed*, instructs the computer to perform various functions. The following claim is a generic example of a proper computer program product claim;

> A computer program product embodied on a computer-readable medium and comprising code that, when executed, causes a computer to perform the following:
>
> Function A
>
> Function B
>
> Function C, etc...

***Claim Interpretations***

6. **The Examiner has given the claims their broadest reasonable interpretation.**

7. The following disclosures are interpreted as *Applicant's Admission regarding prior art*:

- page 2 (first paragraph) is Applicant's Admission regarding prior art teaching of the relationship between drivers and noise and the use of different drivers to counteract the effects of noise;

- page 3, last paragraph, page 9, last paragraph and page 10 are Applicant's admittance regarding the ability of a skilled artisan;

- page 5, (first full paragraph) is Applicant's Admission regarding prior art teaching of curves for various driver circuits of noise amplitude vs. length of lines;

- page 5, (first full paragraph) is Applicant's Admission regarding prior art teaching of the lower susceptibility of wires to noise for stronger drivers;

- page 6, (second paragraph - lines 1-4) is Applicant's Admission regarding prior art teaching of criterion for noise levels.

## *Claim Rejections - 35 USC § 102*

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

**9. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Jones et al..**

- Jones et al. disclose ***automated cost-based placement*** (wherein ***cost*** includes timing and ***noise***) of library cells (including buffers) and the use of Design Rule checking (DRC). See: abstract; fig. 1-3, fig. 4 (cell library and speed paths), fig. 5 (timing); col. 1-2 (general background); col. 3, lines 29-65 (details about the placement, cost function, cell library, speed, ***noise***); col. 5, lines 47-60 (cell library, buffers); col. 6, lines 36-47 (goals of optimized placement); col. 7, lines 3-43 (cost and iteration); col. 8, lines 9-42 (***goals of optimized placement***); col. 9-10

(automated, iterative, cost-based layout; timing, ***noise***; DRC). ***Jones et al. teaches noise avoidance as one of many criteria for optimal cell placement.***

**10. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Alpert et al. (6,117,182) or Dwyer et al..**

- ***Alpert et al. ( '182)*** disclose a method for ***optimal insertion of buffers into an integrated circuit design***. A model representative of a plurality of circuits is created where each circuit has a receiving node coupled to a conductor and a source. A receiving node is selected from the modeled plurality of circuits and circuit noise is calculated for the selected receiving node utilizing the circuit model. ***If the calculated circuit noise exceeds an acceptable value an optimum distance is computed from the receiving node on the conductor for buffer insertion.*** In a multi-sink circuit merging of the noise calculation for the two receiving circuits must be accomplished. ***If an intersection of conductors exists between the receiving node and the optimum distance a set of candidate buffer locations is generated. The method then prunes inferior solutions to provide an optimal insertion of buffers***. See fig. 3-6. See entire disclosure.

- ***Dwyer et al.*** disclose a method (and a system for using the method) for ***placing a semiconductor circuit device between a driver and one or more receivers on the floor space of a chip***. The method includes the steps of: determining respective distances between the driver and each of the one or more receivers; determining a shortest of the distances; determining midpoint along the shortest distance; determining whether the midpoint is predesignated to the floor space of one or more blocking semiconductor circuit devices; ***placing the repeater at the midpoint if***

***the midpoint is not predesignated to the one or more blocking semiconductor circuit devices; and applying a backoff algorithm to incrementally back away from the midpoint to an optimal location, and placing the repeater at the optimal location, if the midpoint is predesignated to the one or more blocking semiconductor circuit devices.*** The method can also include the steps of: determining whether the to be placed semiconductor circuit device can be placed at a set of incremental locations located along one or more axes away from the midpoint; and placing the to be placed semiconductor circuit device at one of the one or more acceptable incremental locations. The step of determining the set of incremental locations can be performed in a spiral pattern away from the midpoint. ***The semiconductor circuit device to be placed can be, for example, a repeater along the path of a net (length of wire) to regenerate a propagated signal.***

## *Claim Rejections - 35 USC § 103*

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham v. John Deere Co.*, 148 USPQ 459, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or unobviousness.

**13. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over [Jones et al. or Alpert et al. (6,117,182) or Dwyer et al.] in view of Applicant's Own Admission.**

- Jones et al. disclose ***automated cost-based placement*** (wherein ***cost*** includes timing and ***noise***) of library cells (including buffers) and the use of Design Rule checking (DRC). See: abstract; fig. 1-3, fig. 4 (cell library and speed paths), fig. 5 (timing); col. 1-2 (general background); col. 3, lines 29-65 (details about the placement, cost function, cell library, speed, ***noise***); col. 5, lines 47-60 (cell library, buffers); col. 6, lines 36-47 (goals of optimized placement); col. 7, lines 3-43 (cost and iteration); col. 8, lines 9-42 (***goals of optimized placement***); col. 9-10 (automated, iterative, cost-based layout; timing, ***noise***; DRC). ***Jones et al. teaches noise avoidance as one of many criteria for optimal cell placement.***

- ***Alpert et al. ( '182)*** disclose a method for ***optimal insertion of buffers into an integrated circuit design***. A model representative of a plurality of circuits is created where each circuit has a receiving node coupled to a conductor and a source. A receiving node is selected from the modeled plurality of circuits and circuit noise is calculated for the selected receiving node utilizing the circuit model. ***If the calculated circuit noise exceeds an acceptable value an***

***optimum distance is computed from the receiving node on the conductor for buffer insertion.*** In a multi-sink circuit merging of the noise calculation for the two receiving circuits must be accomplished. ***If an intersection of conductors exists between the receiving node and the optimum distance a set of candidate buffer locations is generated. The method then prunes inferior solutions to provide an optimal insertion of buffers***. See fig. 3-6. See entire disclosure.

- ***Dwyer et al.*** disclose a method (and a system for using the method) for ***placing a semiconductor circuit device between a driver and one or more receivers on the floor space of a chip***. The method includes the steps of: determining respective distances between the driver and each of the one or more receivers; determining a shortest of the distances; determining midpoint along the shortest distance; determining whether the midpoint is predesignated to the floor space of one or more blocking semiconductor circuit devices; ***placing the repeater at the midpoint if the midpoint is not predesignated to the one or more blocking semiconductor circuit devices; and applying a backoff algorithm to incrementally back away from the midpoint to an optimal location, and placing the repeater at the optimal location, if the midpoint is predesignated to the one or more blocking semiconductor circuit devices.*** The method can also include the steps of: determining whether the to be placed semiconductor circuit device can be placed at a set of incremental locations located along one or more axes away from the midpoint; and placing the to be placed semiconductor circuit device at one of the one or more acceptable incremental locations. The step of determining the set of incremental locations can be performed in a spiral

pattern away from the midpoint. ***The semiconductor circuit device to be placed can be, for example, a repeater along the path of a net (length of wire) to regenerate a propagated signal.***

14. (Jones et al. or Alpert et al. or Dwyer et al.) do not disclose replacement of drivers.

**15. Applicants have admitted the following:**

- page 2 (first paragraph) is Applicant's Admission regarding prior art teaching of the relationship between drivers and noise and the use of different drivers to counteract the effects of noise;

- page 3, last paragraph, page 9, last paragraph and page 10 are Applicant's admittance regarding the ability of a skilled artisan;

- page 5, (first full paragraph) is Applicant's Admission regarding prior art teaching of curves for various driver circuits of noise amplitude vs. length of lines;

- page 5, (first full paragraph) is Applicant's Admission regarding prior art teaching of the lower susceptibility of wires to noise for stronger drivers;

- page 6, (second paragraph - lines 1-4) is Applicant's Admission regarding prior art teaching of criterion for noise levels.

16. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of (Jones et al. or Alpert et al. or Dwyer et al.) to modify the drivers for the following reasons:

- There are two techniques in this art to solve the noise problem - increase the driver strength and insert buffers. Both were extremely well known in the art at the time of the

invention. Applicants have admitted (first paragraph, page 2) that it was known to "*...increase the size of the driver supplying signals to a conductive path which is deemed to be noise sensitive.*". Applicanrs have also admitted (first full paragraph, page 5) that "*It is well known that a conductive path of a given length being driven by a weak driver will have a higher susceptibility to noise than that same conductive path when driven by a stronger driver.*" Clearly, if increasing the buffer strength is not sufficient to solve the noise problem, then buffers would *also* be required.

## ***Conclusion***

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- ***Alpert et al. ('209)*** disclose a method and system for ***segmenting wires in the design stage of a integrated circuit to allow for the efficient insertion of an optimum quantity of buffers***. The method begins by locating wires in the integrated circuit which interconnect transistors and then determining the characteristics of the transistor and the characteristics of the interconnecting wires. ***Next, the method computes a first upper limit for an optimum quantity of buffers utilizing total capacitive load wire and transistor characteristics, then the method computes a second upper limit for an optimum quantity of buffers assuming buffer insertion has decoupled the capacitive load***. Finally, the method segments the wires by inserting nodes utilizing the greater of the first computation or the second computation. ***A determined upper limit on buffer quantity allows wires to be segmented such that the number of candidate***

***buffer insertion topologies is manageable. Therefore, an optimum number of buffers can be efficiently inserted by buffer insertion method which utilize the segmented wires***. See entire disclosure.

- ***Shah et al.*** disclose "*Wiresizing with buffer placement and sizing for power-delay tradeoffs.*" They further disclosethat, with the increasing influence of the resistive effects of interconnects on the performance of VLSI systems, a greater stress is being laid on careful interconnect design. One prominent technique is the approach of sizing wires for long interconnects to achieve the desired speed and power characteristics. It has also been suggested that one may appropriately insert repeaters for significant delay reductions. This paper unifies these approaches to optimizing an interconnect by placing a prespecified number of buffers (drivers and repeaters) using a dynamic programming procedure and then performing simultaneous wire and buffer sizing using a sensitivity-based heuristic. Experimental results are presented to prove the utility and performance of the approach.

- ***Lillis et al.*** disclose "*Optimal wire sizing and buffer insertion for low power and a generalized delay model.*" They further disclose present efficient, optimal algorithms for timing optimization by discrete wire sizing and buffer insertion. Our algorithms are able to minimize a cost function subject to given timing constraints; we focus on minimization of dynamic power dissipation, but the algorithm is also easily adaptable to, for example, area minimization. In addition, the algorithm efficiently computes the complete, optimal power-delay trade-off curve for added design flexibility. An extension of our basic algorithm accommodates a generalized delay

model which takes into account the effect of signal slew on buffer delay which can contribute substantially to overall delay. To the best of our knowledge, our approach represents the first work on buffer insertion to incorporate signal slew into the delay model while guaranteeing optimality. The effectiveness of these methods is demonstrated experimentally.

- ***Dhar et al.*** disclose "*Optimum buffer circuits for driving long uniform lines.*" They further disclose the design of optimum buffer circuits for driving long uniform lines is discussed. Given a uniform line, the size of the buffer driving the line, and the value of the capacitive load driven by the line, the problem considered consists of determining the type, number, and position of buffers that minimize the delay in the line. A variation of this problem that is also considered consists of minimizing the delay in the line when the area occupied by the buffers is constrained; this leads to the solution of the problem of minimizing the delay in driving a pure capacitive load under buffer area constraint. The optimal solution is formally developed, and some very good approximate solutions that can be obtained via simple computations are presented. It is shown that accepting a small increase in delay (of usually 5% over the minimum) can lead to a significant (about 50%) decrease in the area occupied by the buffers. Design curves that allow the reader to determine the optimum buffers with little effort are presented.

- ***Sato et al.*** disclose in an automated design, a useful insertion of a delay buffer or an increase in the delay time of the critical path could not been prevented. When inserting a logic element between two certain points on the circuit, substitution of other paths passing through the

relevant insertion position is considered and the insertion position of the logic element is determined finally.

- ***Kuroda*** teaches (abstract): "In a layout system of a logic circuit, a buffer inserted into a critical path is arranged/wired in an arranged region of a circuit block of a primitive layout in such a manner that delay time of the critical path in the primitive layout can be limited to an allowed value. ..." See: abstract; fig. 3, 6 (buffer arranging); col. 1, line 10 to col. 2, line 44 (buffer insertion and timing considerations); col. 3, line 46 to col. 8, line 9 (details of buffer arranging and its effect on timing).

- ***Schaefer et al.*** teaches a design methodology for designing a buffer circuit that meets specified timing constraints, without making the circuit larger than required. See: abstract; fig. 3 (buffer tree), 4, 7 (slack), 9; col. 1, line 7 to col. 4, line 17 (prior art teaches details of buffer arrangement as per timing considerations); col. 4, lines 20-57 (interactive buffer insertion and deletion with timing constraints); col. 6, line 41 to col. 7, line 54 (placement algorithm); col. 11, line 1 to col. 13, line 68 (slack).

- ***McClure*** teaches details of buffers, crosstalk and noise suppression. See: abstract; fig. 1 and 3-5; col. 1, line 21 to col. 2, line 3 (teaches that noise was a well known problem); col. 2, lines 6-43 (teaches that it was well known to use buffers to solve noise problems).

- ***Drumm et al.*** disclose a simple system and method that provides for the identification and removal of unnecessary buffers in a logic circuit. A special pseudo-buffer is added to the library and identified as a buffer cell with zero area. In addition, a feedthrough delay rule is

associated with the pseudo-buffer such that it is treated by a timing system as a wire with no delay through which all electrical properties pass. An existing repowering function will then consider the pseudo-buffer as a replacement choice when attempting to select an optimal power level. If the pseudo buffer is chosen, it can be easily removed from the circuit at some time thereafter.

- ***Alpert et al.*** disclose "*Buffer insertion for noise and delay optimization.*" They further disclose that buffer insertion has successfully been applied to reduce delay in global interconnect paths: however, existing techniques only optimize delay and timing slack. With the increasing ratio of coupling to total capacitance and the use of aggressive dynamic logic circuit families, noise is becoming a major design bottleneck. They present comprehensive buffer insertion techniques for noise and delay optimisation. Their experiments on a microprocessor design show that our approach fixes all noise violations that were identified by a detailed, simulation-based noise analysis tool. Further, we show that the performance penalty induced by optimizing both delay and noise as opposed to only delay is 2%.

- ***Culetu et al.*** disclose "*A practical repeater insertion method in high speed VLSI circuits.*" they further disclose that, in today's design of VLSI high speed circuits, frequency has a major impact on the number of repeaters that needs to be inserted. A microprocessor operating at less than 200 Mhz might require several hundred repeaters, while one operating at greater than 500 Mhz may require a number in the thousands. The following paper describes an efficient and simple way to automatically determine buffer placement based on maintaining equal transition time for all gate input signals across the net. A maximum allowable transition time is determined

(limited by the frequency of the circuit), and correlated with the interconnect Elmore Delay. A Spice RC model having nodes with physical locations (X, Y coordinates) can be obtained by extraction tools providing standard parasitic format (SPF). This can then be used with the results of the algorithm for repeater placement to determine the exact physical location desired for each repeater.

- ***Cong*** discloses "*Modeling and layout optimization of VLSI devices and interconnects in deep submicron design.*" Cong further discloses an overview of recent advances on modeling and layout optimization of devices and interconnects for high-performance VLSI circuit design under the deep submicron technology. First, they review a number of interconnect and driver/gate delay models, which are most useful to guide the layout optimization. Then, they summarize the available performance optimization techniques for VLSI device and interconnect layout, including driver and transistor sizing, transistor ordering, interconnect topology optimization, optimal wire sizing, optimal buffer placement, and simultaneous topology construction, buffer insertion, buffer and wire sizing. The efficiency and impact of these techniques will be discussed in the tutorial.

**18. Any inquiry concerning this communication or earlier communications from the examiner should be:**

**directed to:**

Dr. Hugh Jones telephone number (703) 305-0023, Monday-Thursday 0830 to 0700 ET, ***or*** the examiner's supervisor, Kevin Teska, telephone number (703) 305-9704. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

**mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

**or faxed to:**

(703) 308-9051 (for formal communications intended for entry)

***or*** (703) 308-1396 (for informal or draft communications, please label "*PROPOSED*" or "*DRAFT*").

Dr. Hugh Jones

January 31, 2002

DR. HUGH M. JONES
PATENT EXAMINER
ART UNIT 2123